MAXIM Engineering Journal

News Briefs

JANUARY 27, 1993

Maxim UK is continuing to invest in the services that our engineering-oriented customers require. Our leadtimes are now among the best in the analog industry, thanks to an increase in inventory over the past few months. New product samples and literature are available within 24 hours. We strive to ensure that engineers have the information on their desk when they need it.

Maxim UK has just concluded its 1993 seminar series with a record number of attendees. Evaluations reflect that the seminars were very positively received by British engineers. If you would like a copy of the information distributed at the seminar – the *1993 New Releases Book* and the *1993 Applications Handbook* – you may request them by phone or FAX. If you would like free samples, data sheets, or back issues of the *Engineering Journal*, just phone us on (0734) 845225, FAX us on (0734) 843863, or contact us on our new Free Phone number, (0800) 585048.

Maxim UK looks forward to continuing our mutually beneficial relationship with the engineering community. Our twenty plus staff is anxious to offer solutions for your technical challenges.

MAXIM CERTIFIED TO OZONE-DEPLETING CHEMICALS (ODC) STANDARD

Chlorofluorocarbon (CFC) and Ozone Depleting Chemical (ODC) elimination have been a high priority for all facets of Maxim's manufacturing processes, even before the Montreal Protocol was issued with a May 15, 1993 compliance deadline. Maxim's fabrication facility and shipping methods already conform, and product assembly will soon follow. Official certification of compliance is expected in early 1993.

HAST TESTING SPEEDS PRODUCT QUALIFICATION

Maxim can now bring new products to market quicker while maintaining their high quality standards thanks to HAST (Highly Accelerated Steam and Temperature) testing. HAST testing replaces the commonly-used moisture tolerance test called 85°C/85 RH to measure plastic product performance in a moist environment. This new testing technique reduces test time to 100 hours, compared to 1,000 hours for old test methods, which provides process engineers with immediate feedback to manufacturing changes. HAST testing uses 125°C and elevated pressure with a constant humidity level of 85%.

FABRICATION PROCESS DECREASES FAILURE RATE

Maxim is making products more reliable by significantly reducing long-term and infant-mortality failure rates — long-term measures potential field failure rates, while infant mortality measures a manufacturer's in-process failure rate. Maxim achieves a low 2.63 FIT long-term rate, and a 186 PPM infant mortality rate by improving their consistency and basic processing integrity, down from 4.63 FIT long-term, and 256 PPM infant mortality.

Serial-Data Transmission with Maxim ICs

Serial transmission provides a simpler, lower-cost interface for modest-bit-rate applications

Serial transmission offers advantages over the parallel transmission of digital data for bit rates as high as 3 or 4 Mbps. Parallel is faster, but serial is more attractive for moderate to long distance. It requires less wire, less hardware, and less critical timing. Even if signals remain on the board, serial transmission requires less area and fewer pins on the ICs. At issue for product designers is the choice among several well-established protocol standards for serial-data transmission. Which to follow?

Maxim's standard interface for serial-data ICs provides hardware specifications common to the existing synchronous standards. Most Maxim parts are therefore compatible with a majority of the established synchronous-serial standards: Motorola's SPI and QSPI, National Semiconductor's Microwire, and others from Hitachi, Intel, and Texas Instruments.

The following discussion acquaints readers with the mechanics of serial-data transmission, and explains how serial-interface ICs may be connected to existing synchronous-transmission ports. Points are illustrated with a typical application.

Synchronous vs. asynchronous transmission

RS-232 is the best-known standard for asynchronous serial transmission. Currently known as EIA-232-E, it specifies signal-waveform parameters, signal lines (one each for transmit, receive, and ground, plus certain other auxiliary functions), and mechanical dimensions for the 25-pin connectors that terminate the signal cable. None of this information, however, enables the hardware to interpret received data. That job is accomplished by applications software, which inserts non-data pulses—start, stop, and parity bits—in the transmitter's data stream.

Those unfamiliar with serial-data transmission may assume that synchronous and asynchronous data transceivers are similar, and that changing one to the other involves little more than rearranging a few external logic gates. That assumption often leads to the question "How do I connect my synchronous-serial A/D converter to an (asynchronous) RS-232 port?"

It's not practical, is the answer. A synchronous-to-asynchronous interface requires lots of circuitry: either a microcontroller, or a shift register and UART (universal asynchronous receiver-transmitter) controlled by a PAL or discrete-logic state machine. The fact that RS-232 is "serial," therefore, is no reason to choose a serial A/D converter. Most serial A/D converters are inherently incompatible with the RS-232 lines.

You may need a serial A/D converter for other reasons: fewer data lines can lower the cost of galvanic isolation or simplify the hookup to remote locations, for example. Otherwise, it makes more sense to feed an RS-232 port with a parallel-output A/D converter!

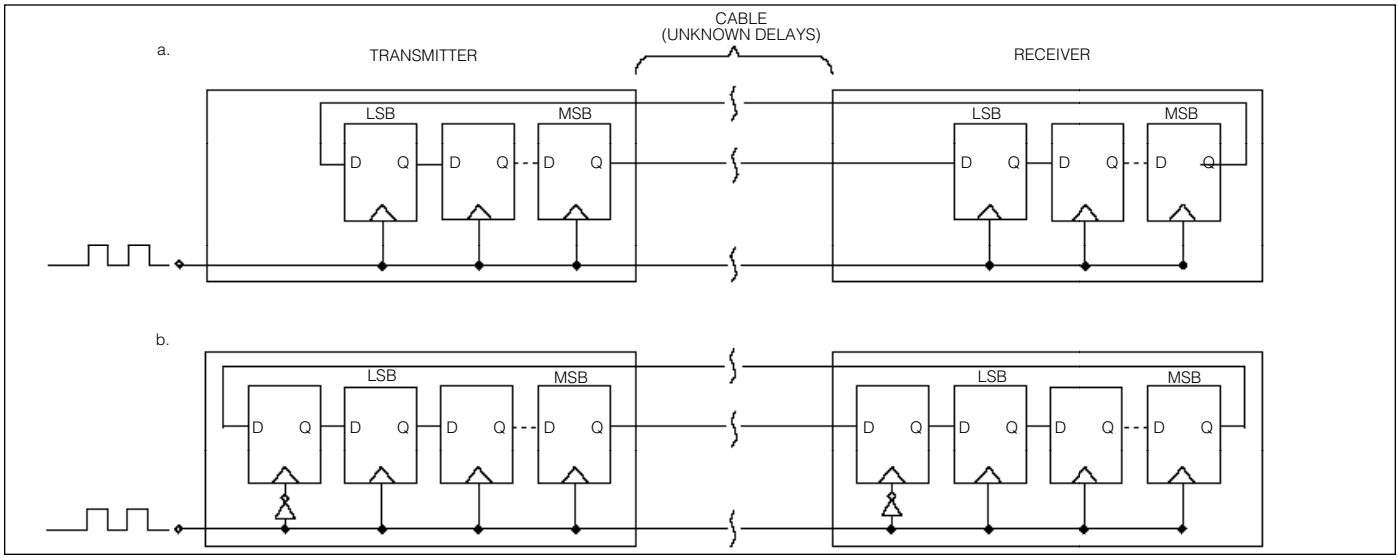

Figure 1. *In a bare-minimum synchronous-serial communications system (a), the clock drives identical shift registers at either end of the cable. Adding a flip-flop and inverter to the registers (b) allows each interface to latch input data and shift output data on opposite clock edges, thereby extending the allowable load capacitance and cable length.*

Data transmission vs. laundry

In its simplest form, a synchronous-transmission protocol similar to SPI or Microwire requires two shift registers connected as a continuous ring counter, one local and one at the far end of the cable (**Figure 1a**). The system then behaves like a pulley-supported washline between two tenement buildings—for every foot of line you shift out toward the other building, you must accept one foot of line from the other side. Similarly, for every bit of data you transmit via this (highly simplified) synchronous interface, you must accept one bit of data (or garbage) from the other end.

Synchronous transmission is so named because the transmitter provides a clock signal, separate from the data signal, and synchronizes the midpoint of each data bit with a clock transition. Clock and data lines are separate. The clock signal enables each receiver to sense incoming data bits without the overhead of start, stop, and parity bits required in asynchronous transmission. This "serial clock" is not continuous; it operates only when data is actually transmitted.

With these basics in mind, consider a shortcoming of the simplified diagram of **Figure 1a**: it makes no allowance for unequal delays in the cable. At the receiver end, these time skews between the clock and data waveforms can garble transmissions by eating up the required data-hold time. The simple connection, therefore, is reliable only if you can guarantee that cable skew will never exceed the net effect of transmitter propagation delay and receiver hold time.

The skew problem is easily solved with an additional flip-flop and inverter preceding each shift register (**Figure 1b**). The additional flip-flop allows data to be sampled and shifted on opposite-polarity edges. This arrangement extends the receiver's data-hold time to a half clock cycle minus the cable skew—more than enough margin for most systems (**Table 1**).

Table 1—Setup and Hold Specifications

	Max Setup (ns)	Max Hold (ns)
Maxim's serial interface	<100	0
SPI	100	100
Microwire	100	100

Note also that the shift registers are depicted as "D-type" flip-flops in cascade. The D types yield simple diagrams, but R-S flip-flops are required in practical data-transmission systems because their Preset and Clear inputs allow rapid loading of parallel data.

Different protocols; different standards

Figure 2 summarizes the protocol options available with SPI and other standards. This diagram shows the four possible

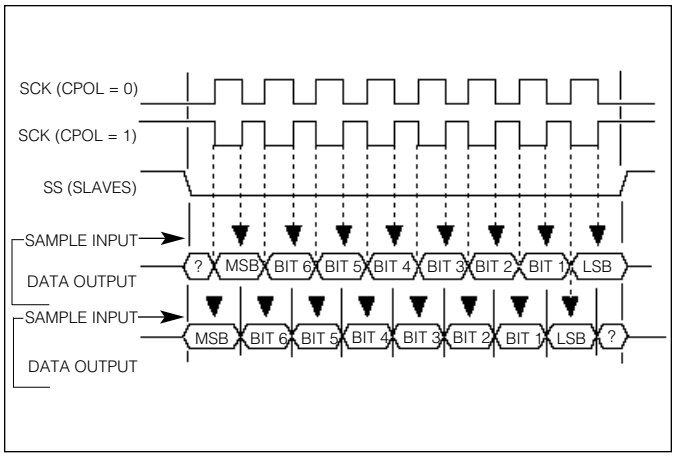

***Figure 2**. This diagram shows the four transmission protocols that derive from a two-state clock polarity and two-state clock phase: (CPOL=0, CPHA=0), (CPOL=0, CPHA=1), (CPOL=1, CPHA=0), and (CPOL=1, CPHA=1).*

relationships between clock and data, given a clock polarity that is initially high (CPOL=1) or initially low (CPOL=0), and a clock phase such that data is sampled on the first edge of a transmission (CPHA=0) or the second edge (CPHA=1). Motorola's synchronous peripheral interface (SPI) lets you program any of these four protocols.

The device that generates the serial clock is designated "master" whether it transmits or receives, and all other devices on the serial bus are referred to as "slaves." Motorola's SPI lets you program each interface to be master or slave, but like most synchronous serial standards it accommodates only one master in a system. SPI commits the system to 8-bit transfers, MSB first.

Motorola also offers an enhanced version of SPI called QSPI, for Queued SPI. Microcontrollers with QSPI provide the full SPI capabilities, plus a micro-sequencer and small RAM for storing up to 16 data entries. While maintaining this queue of information, the micro-sequencer can simultaneously control four peripherals without taxing the CPU, or 16 peripherals with the addition of a 4-line decoder.

QSPI enables a master to scan the slave devices while maintaining a record of the most-recent transaction with each. This record consists of a transmit word, a receive word, and a control byte that customizes each transaction according to the needs of that peripheral: four bits comprise a slave-select code, and the other four specify timing delays and a word length of eight to sixteen bits. For a given entry, the transmit and receive words must have the same length.

The Microwire standard from National Semiconductor is similar to SPI but less flexible. It also commits the system to 8-bit transfers, along with CPOL=0 clock polarity, CPHA=0 clock phase, and a single master (Microwire/Plus equals Microwire plus the CPHA=1 option).

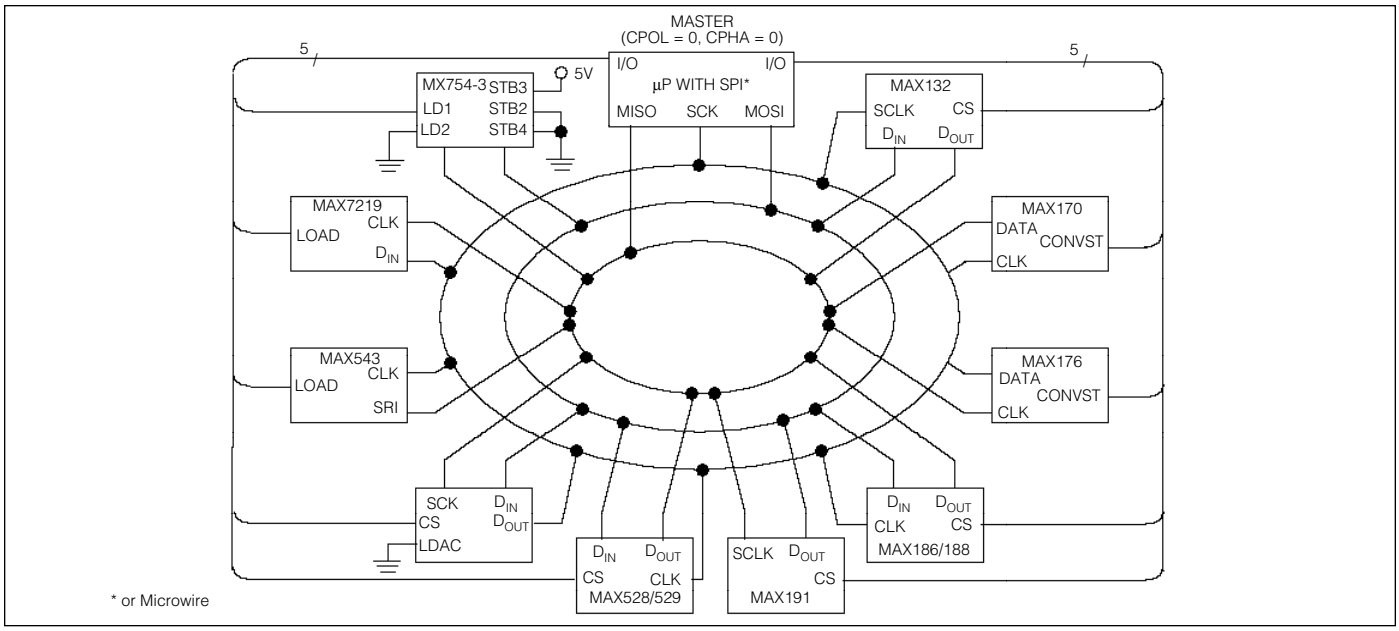

Figure 3. *All synchronous-serial ICs from Maxim can operate on a common serial interface as shown except the MAX121 A/D converter and the MAX500 quad D/A converter, which are compatible with SPI and QSPI but not Microwire. Only the MAX191 and MAX532 comply fully with Maxim's new synchronous-serial standard.*

Maxim offers a variety of serial-interface products that connect directly to SPI, QSPI, and Microwire serial buses without additional hardware. These products include A/D converters, D/A converters, and LED display drivers.

Maxim's standard

Maxim's own synchronous-serial standard complies electrically with Microwire but differs in the pin names (**Table 2**). Like Microwire, the Maxim serial interface samples (receives) data on rising edges of the clock and shifts (transmits) data on falling edges.

Because Microwire is a subset of Microwire/Plus and of Motorola's SPI, products with a Maxim Serial Interface (MSI) are compatible with these and other systems. Future synchronous-serial products from Maxim will meet the MSI standard unless that compliance conflicts with the product's intended application.

Table 2—Pin Name Comparison

	Maxim	SPI/QSPI	Microwire
Serial Clock Output	SCLK	SCK	SK
Serial Data Input	DIN	MISO	SI
Serial Data Output	DOUT	MOSI	SO

Figure 3 shows a system compatible with Maxim's serial interface, in which a microprocessor (the master) controls ten synchronous-serial ICs with the help of 10 programmable I/O lines. The µP can be equipped with the Microwire interface, or with an SPI or QSPI interface programmed for CPOL=0, CPHA=0. These ten ICs (**Table 3**) require no additional hardware, but some require different software routines (**Table 4**).

Table 3—Maxim Products with a Synchronous-Serial Interface

MAX132	18-bit integrating A/D converter
MAX170	12-bit successive-approximation A/D converter with reference
MAX176	High-speed, 250ksps, 12-bit A/D converter with track/hold and reference
MAX186/188	8-channel, 12-bit, single-supply, data-acquisition system with track/hold and reference
MAX191	12-bit, single-supply A/D converter with track/hold and reference
MAX528/529	Octal, 8-bit, voltage-output D/A converter
MAX532	Dual 12-bit voltage-output D/A converter
MAX543	12-bit current-output D/A converter
MAX7219	LED display driver
MX7543	12-bit current-output D/A converter

The MAX190 is a 12-bit A/D converter similar to the MAX191. Both devices include a track/hold, reference, differential inputs, and parallel as well as serial outputs. The MAX190 guarantees a 76ksps throughput and the MAX191 guarantees 100ksps. To understand a typical serial interface, consider the requirements for connecting the MAX190 to an SPI or Microwire port.

Motorola's MC68HC11 microcontroller (µC) is typical of devices offering an SPI port. It connects to the MAX190 via three wires and no additional hardware (**Figure 4**). Two software routines complete the interface. The first (**Listing 1**) programs the µC's clock polarity (CPOL=0), clock phase (CPHA=0), chip-select line (bit 0 of port B), and transmission rate (one half the internal "E" clock frequency). The second routine (**Listing 2**) triggers an A/D conversion and stores it in the µC's "D" register.

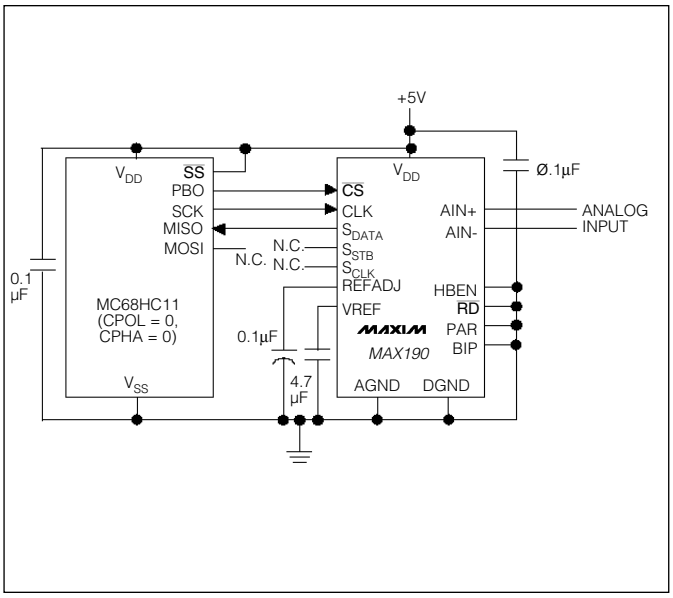

Figure 4. *The physical interface between an SPI (or Microwire) master and the MAX190 A/D converter is simply three direct connections. Software routines complete the interface. The MAX190 pins* CS, *CLK,* S_{DATA}, *and* S_{STB} *correspond to MAX191 pins* CS, *SCLK, DOUT, and SSTRB.*

When CS goes low, the MAX190 initiates a conversion by switching its track/hold to hold. The next 13 clock cycles complete the conversion by shifting out 13 bits from the S_{DATA} pin, MSB first (after one leading zero). Additional clock edges cause the converter to shift out trailing zeros.

The µC acquires MAX190 data in two 8-bit SPI transfers, which arrive as a leading zero, 12 bits of data, and three trailing zeros (**Figure 5**). After transferring these to its 16-bit D register, the µC eliminates the trailing zeros by performing three right shifts.

Table 4 —General Software Techniques for Special Signals

CS	The internal shift register does not transmit or receive data until CS is brought low, and data in the shift register is latched to other internal registers when CS is brought high. When CS is high, the serial output assumes a high-impedance state. 1. Pull CS low. 2. Transfer eight bits of serial data (MAX132), or 16 bits (MAX186, 188, 191, 528, 529), or 24 bits (MAX186, 188, 532). 3. Bring CS high.
LOAD; LDAC	Data entering the shift register is not latched to internal registers until LOAD or LDAC goes low. (The MX7543's LD1 terminal functions as LOAD when LD2 is grounded.) 1. Transfer 16 bits of serial data (MAX543, MX7543). 2. Pull LOAD low. 3. Bring LOAD high.
LOAD	Data entering the shift register is not latched to internal registers until LOAD exhibits a rising edge. 1. Transfer 16 bits of serial data (MAX7219). 2. Bring LOAD high. 3. Pull LOAD low.
CONVST	A rising edge on CONVST initiates an A/D conversion. CONVST should be brought high, then low, followed by the serial transmission of 16 clock cycles. The first two and the last two cycles generate garbage bits because DATA (which feeds MISO) is in the high-impedance state at those times. To remove the four garbage bits, execute an AND instruction with the mask $3FFC and then perform two 16-bit right shifts. 1. Bring CONVST high. 2. Pull CONVST low. 3. Transfer 16 bits of serial data (MAX170, MAX176).

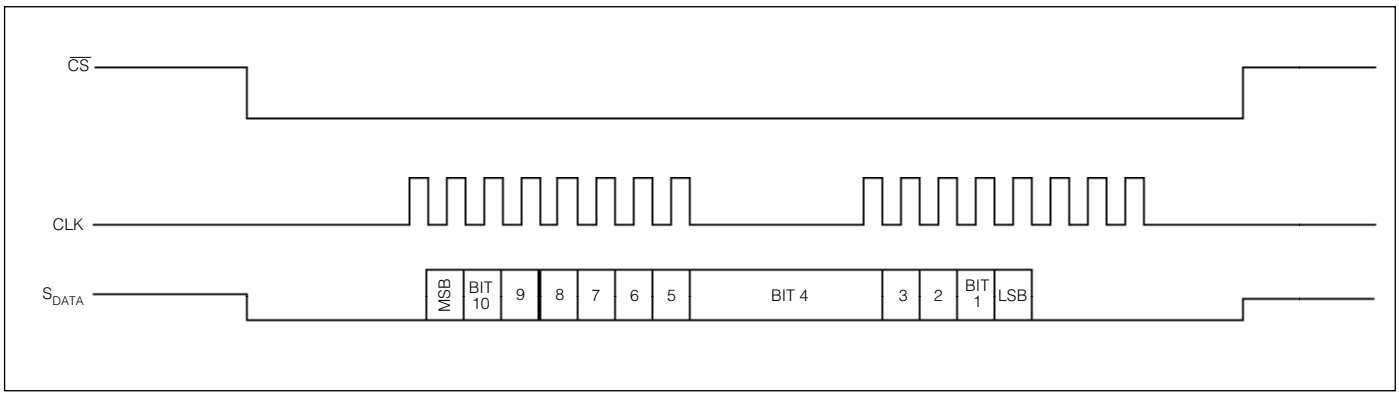

Figure 5. *This timing diagram illustrates an SPI interface for the MAX190 A/D converter.*

Listing 1—Programs the Microcontroller

```
INITSPI
;This routine sets up the SPI port to operate at its full speed
;of one half the system E clock frequency and sets CPOL=0 and
;CPHA=0.  Port B bit 0, PBO, is used to drive the MAX190;s
;CS\ line.
          PSHA                ;SAVE THE A REGISTER
          LDAA      #$01
          ORAA      PORTB
          STAA      PORTB     ;CS\ IS ACTIVE LOW SO DEASSERT PBO
          LDAA      #$01
          ORAA      DDRB
          STAA      DDRB      ;SET PBO TO BE AN OUTPUT
          LDAA      #%01010000
          STAA      SPCR
;SPIE=0,SPE=1,DWOM=0,MSTR=1,CPOL=CPHA=0
          LDAA      SPSR
          LDAA      SPDR      ;CLEAR SPIF IN CASE OF PREVIOUS ERROR
          PULA                ;RESTORE THE A REGISTER
          RTS
```

Listing 2—Controls the A/D Converter

```
READ190
; This routine uses the MAX190 to perform a 12 bit A/D convertion.
; The conversion result is returned in the D register.  The D
; register will contain the following on return from this
; routine :
; D Bits            15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
; A/D Result         0  0  0  0 MSB                              LSB
; The MAX190 CS\ input must be connected to PB0.
; This routine assumes that any other SPI accesses made sure to
; clear the status register (by reading SPSR) when they were done.
          LDAA      #%11111110 .
          ANDA      PORTB
          STAA      PORTB     ;ASSERT CS\
          LDAB      #$00
          STAB      SPDR      ;TRANSMIT A BYTE OF ALL ZEROS
     WAIT190
          LDAA      SPSR
          BEQ       WAIT190   ;WAIT UNTIL TRANSMISSION COMPLETE
          LDAA      SPDR
          PSHA                ;PUSH HALF OF RESULT ONTO STACK
          STAB      SPDR      ;TRANSMIT A BYTE OF ALL ZEROS
```

Convert AC-Line Voltage to an Isolated, Regulated 5V

Operating on ac line voltage, the power supply of **Figure 1** generates an isolated, regulated 5V output capable of producing 40mA. Because the isolation transformer operates at 25kHz, it is much smaller and lighter than equivalent input transformers operating at 60Hz.

The drop across R1/C1 allows a direct connection between IC_1 and the ac line, and R2 limits the current into C1. IC_1—an ac-to-dc converter containing a full-wave rectifier, 12.4V zener, and series output regulator—provides a regulated supply voltage to IC_2. Normally 5V ±4%, this output (V_{REG}) is adjusted to approximately 5.3V by introducing an external divider (R5/R6) in the regulator's feedback path. This feedback regulates the 5V output by sensing changes in IC_2's output voltage (pin 5) and adjusting V_{REG} accordingly.

IC_2 is a step-down switching regulator that normally operates with an external inductor in the flyback mode. In this circuit it operates with a transformer in the forward mode, applying a chopped -5.3V to the transformer primary. The secondary voltage is then half-wave rectified and filtered to produce the 5V output.

Within IC_2 a large, 1Ω PMOS switch connects LX and V+ (pins 5 and 6). The small drop across this switch is compensated by feedback, as is the drop across diode D4. To provide further compensation for the effects of voltage and temperature variations in this diode, a similar diode (D1) is included in series with the feedback network. Because load current flows in D4 but not in D1 the compensation is partial, resulting in finite load regulation.

Diodes D3 and D2 (a 4V zener) clamp the LX output to approximately -5V, which allows flux in the transformer core to reset on every cycle. The resistor divider R3/R4 applies 2V to IC_2's pin 1, which sets the internal oscillator to 25kHz with a 40% duty cycle. R7 provides a continuous load that bleeds off the energy contributed by leakage conductance in the transformer; without R7, the output will rise higher than the desired 5V.

The circuit delivers 0 to 40mA with a drop of less than 250mV (**Figure 2**). To improve the steep drop in voltage near zero load, you can load the output more heavily by lowering the value of R7. For better load regulation you can raise V_{REG}, either by adjusting the R5/R6 ratio or by altering the transformer turns ratio, and obtain the desired output level by adding a linear regulator.

(Circle 1)

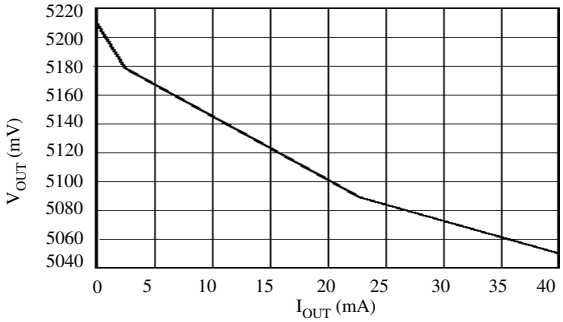

Figure 2. *This graph illustrates output voltage vs. load current for the circuit of Figure 1.*

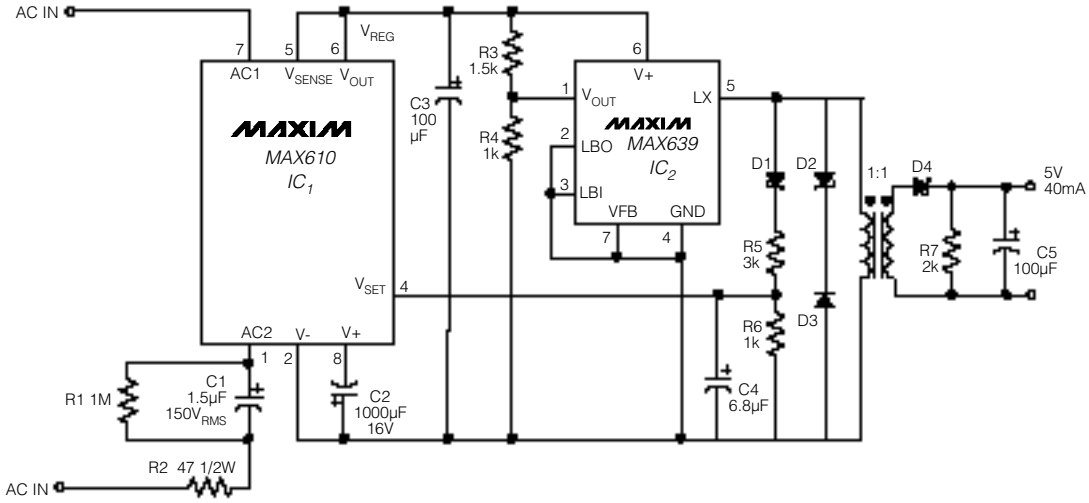

Figure 1. *Driving a transformer at 25kHz, these two ICs derive a regulated 5V output from the ac line voltage.*

Octal Trimpots Offer Rail-to-Rail Adjustments

The octal D/A converter circuit of **Figure 1** operates on 5V and provides eight output voltages, each digitally adjustable from supply rail to supply rail (0 to 5V). Each output has a resolution of 20mV/LSB. The D/A chip (IC_1) requires 3.5V of headroom between its V_{DD} and reference voltages, but a voltage-doubler charge pump (IC_2) removes this limitation by generating an approximate 10V supply for V_{DD}. All the converter references are connected to the 5V supply.

IC_1, which appears as a memory to the controlling µP, draws less than 20mA of quiescent current. IC_2 is a high-current charge pump that normally operates as an inverter. Configured as shown, it doubles the 5V input to an unregulated 10V output and provides an output impedance of less than 10Ω. It can deliver 100mA, which allows the eight D/A converters to issue their maximum output currents simultaneously (8 x 5mA = 40mA).

(Circle 2)

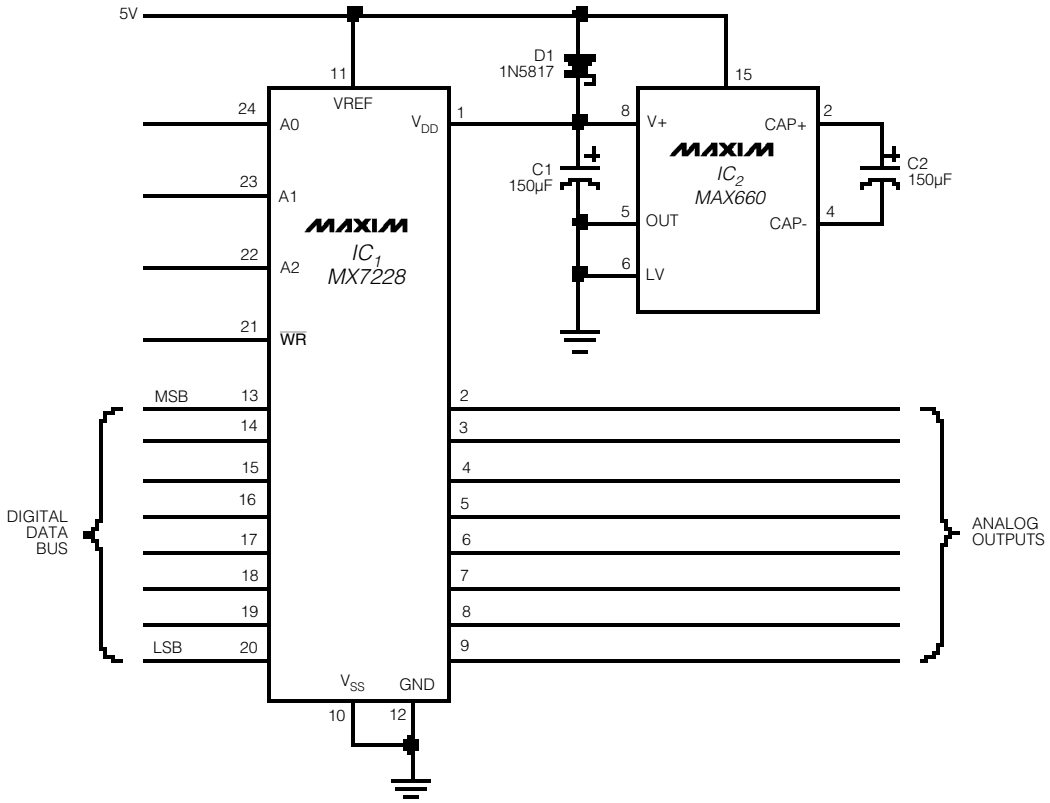

Figure 1. *Because a voltage-doubler charge-pump IC supplies 10V to the octal D/A converters' references, the converter outputs can range from rail to rail (0 to 5V) of the applied supply voltage.*

Remove DC Offset from Lowpass Filters

Adding one more RC network to a lowpass filter **(Figure 1**) restores perfect dc accuracy at the output (otherwise, the output in this case exhibits an offset of about 50mV). You choose R and C for a pole frequency three decades below the filter's cutoff frequency f_C: $1/2\pi RC = f_C/1000$. If desired, the RC output may be buffered with a low-offset op amp as shown. The MAX427, for example, guarantees an offset voltage of 5µV typical (15µV max).

At dc and low frequencies, the dc-accurate output tracks the unfiltered input because R provides a signal path that bypasses the filter. At higher frequencies C begins to conduct, allowing the dc-accurate output to track the filter's lowpass (LPO) output.

Provided the lowpass filter has unity gain and low ripple, the RC network has virtually no effect on filter gain or phase response; the input signal and LPO output swing together throughout most of the passband. Attenuation in the RC filter is sufficient that the active-lowpass filter shape is maintained for frequencies between f_C and the stopband. At higher frequencies, the RC network sets the filter's rolloff rate at 20dB/decade **(Figure 2**).

The RC network slows the process of nulling offsets to zero, but it has no effect on the circuit's response to a step change in the dc input level.

(Circle 3)

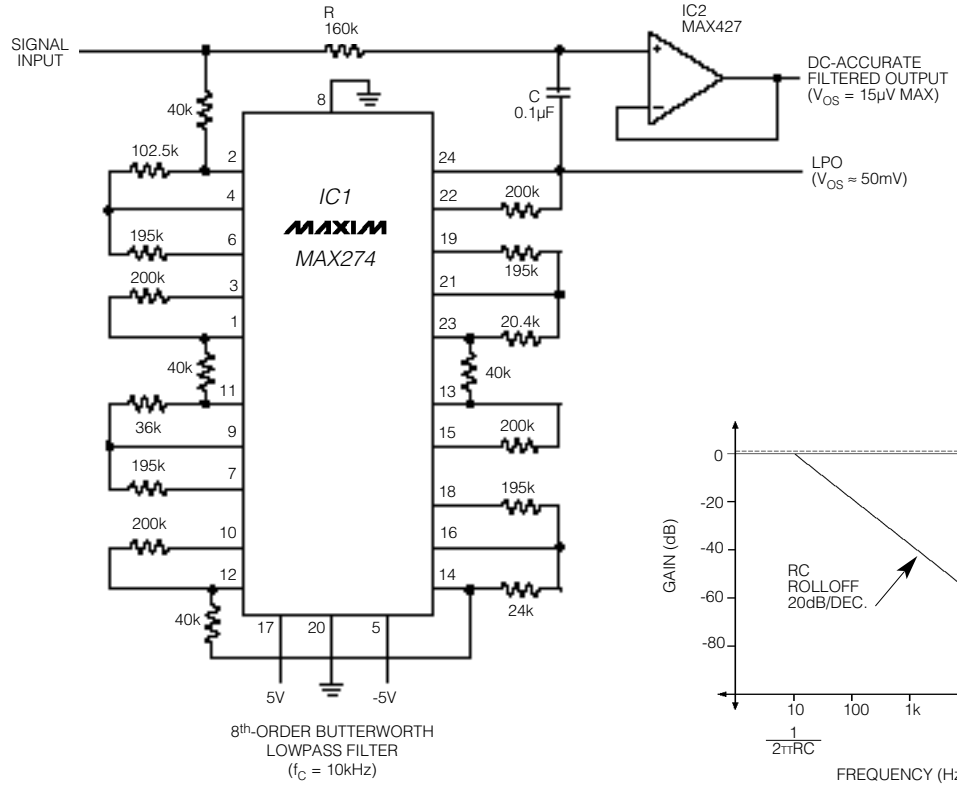

Figure 1. *The external R and C remove dc-offset errors that might otherwise be contributed by the lowpass filter.*

Figure 2. *This Bode plot for the Figure 1 filter shows that the RC network affects frequency response only in the filter's stopband.*

Low-power IC Converts -48V to 5V Without Transformer

To supply small amounts of 5V power in voice- and data-communications hardware, it may be more convenient to derive the voltage from -48V (if available) than to add a separate supply powered by batteries or the ac line. The dc-dc converters of such supplies usually involve expensive modules or discrete components and transformers.

The **Figure 1** circuit is a better choice. For the majority of applications that don't require isolation, this circuit generates 5V @ 150mA without a transformer. The negative input voltage can vary from -35 to -75V.

The switching regulator (IC_1) operates in a classic boost configuration, powered by a zener-regulated 6.3V (relative to -48V). Because its ground terminal connects to -48V, the regulator behaves as if converting 48V to 53V. A feedback signal is level-shifted down from 5V to the IC's feedback input by the transistor current source Q2. Transistor Q3, included only to compensate for the temperature variation of V_{BE} in Q2, can be omitted if approximate 2mV/°C temperature drifts are acceptable.

Conversion efficiency ranges from 70 to 76%, depending on the input voltage and the load. Highest efficiency occurs at full load, when zener current is the lowest percentage of the total supply current. The switching FET (Q1) need not have low on-resistance, because the circuit's supply current is only about 20mA at full load and because the 1Ω sense resistor (R2) limits peak currents to about 200mA.

The device selected for Q1 (a Siliconix 2N7004 in a 4-pin DIP) exhibits a typical $R_{DS(on)}$ of 1Ω when operating with the 6V gate drive provided by this circuit. A SOT-89 surface-mounted FET such as the IRFS1Z0 from International Rectifier also performs well. Rated at 2.4Ω, the IRFS1Z0 reduces efficiency by no more than one or two percentage points. All circuit components in Figure 1 are available in surface-mount versions.

(Circle 4)

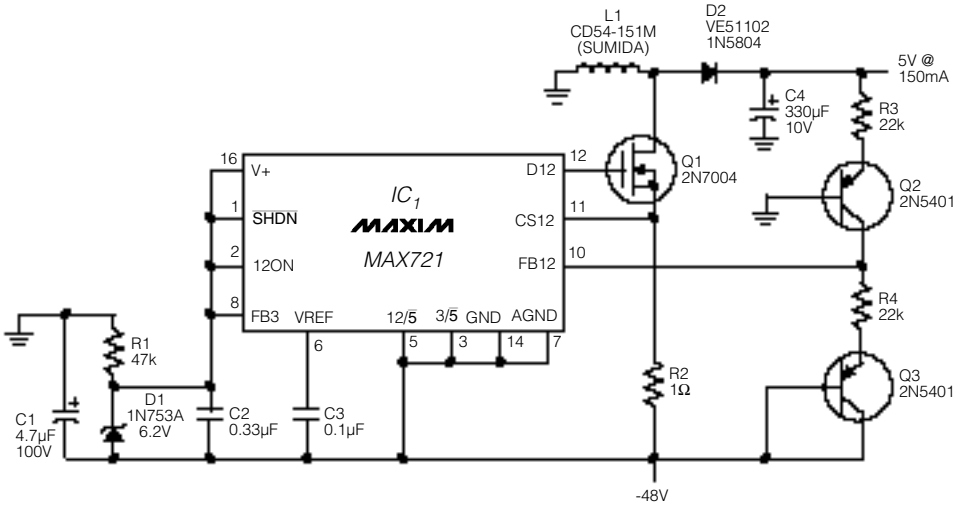

Figure 1. *Unorthodox connections allow this switching-regulator IC to derive 5V @ 150mA from a -48V supply voltage.*

Temperature Compensation Stabilizes LCD Contrast

The variation of LCD contrast with temperature can be a problem in some applications. Working in a meat-packing plant, for instance, you might go from scanning sides of beef in a refrigerated locker to downloading data from your LCD bar-code reader in a heated office. That temperature change would definitely require an LCD-bias adjustment.

Combining automatic bias adjustment with manual-adjust capability lets the user compensate for LCD viewing angles and manufacturing differences (**Figure 1**). This circuit provides a linear bias change with temperature, from -10V at 50°C to -15V at -20°C (**Figure 2**). (IC_1 is a power-supply chip for portable systems that includes two other switching-regulator controllers and four linear-regulator controllers, plus circuitry for backup-battery switchover, low-voltage warning, and power-fail reset.)

The automatic compensation is provided by a negative-temperature-coefficient resistor (R5) that affects the feedback for the V6 regulator in IC_1. Decreasing temperature, for instance, causes an increase in R5's resistance and a consequent increase in the LCD bias voltage (V6). R_4 linearizes the effect of R5, and R3 adjusts the temperature coefficient of R5 to that of the LCD. (Other tempcos require different values for R_2 and R_3.)

To calculate R2 and R3, note that V6 is a function of $V_{D/A}$ and RT. $V_{D/A}$ is the output of the internal 5-bit D/A converter, which allows the user to digitally adjust the LCD bias voltage, and RT is the sum of R3 and the parallel combination of R4 and R5:

$$V6 = V_{D/A} - \frac{(5V - V_{D/A})RT}{R2}$$

$$\text{therefore } R_T = \frac{R2(V_{D/A} - V_6)}{(5V - V_{D/A})}$$

Solve for R_T at the extremes of V6 (-10V and -15V) using the midrange value for $V_{D/A}$ (0.625V):

V6 = -10V: $R_T = 2.43R2$

V6 = -15V: $R_T = 3.57R2$

Equivalent expressions for R_T are based on its definition:

V6 = -10V: $R_T = R3 + (R5\ @50°C) \parallel R4$

V6 = -15V: $R_T = R3 + (R5\ @-20°C) \parallel R4$

From the R5 data sheet, R4 = 277kΩ (choose 280k, 1%), R5 @50°C = 52.7kΩ, and R5 @-20°C = 250.1kΩ. Substitute these values above, equate corresponding expressions for R_T, and solve for R2 and R3:

R2 = 172kΩ (use 169kΩ, 1%).

R3 = 365kΩ (use 365kΩ, 1%).

(Circle 5)

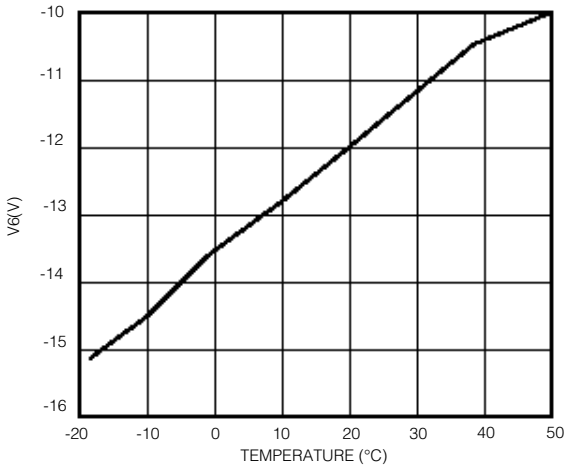

Figure 2. *The regulator output in Figure 1 serves as a temperature-compensated bias voltage for LCDs.*

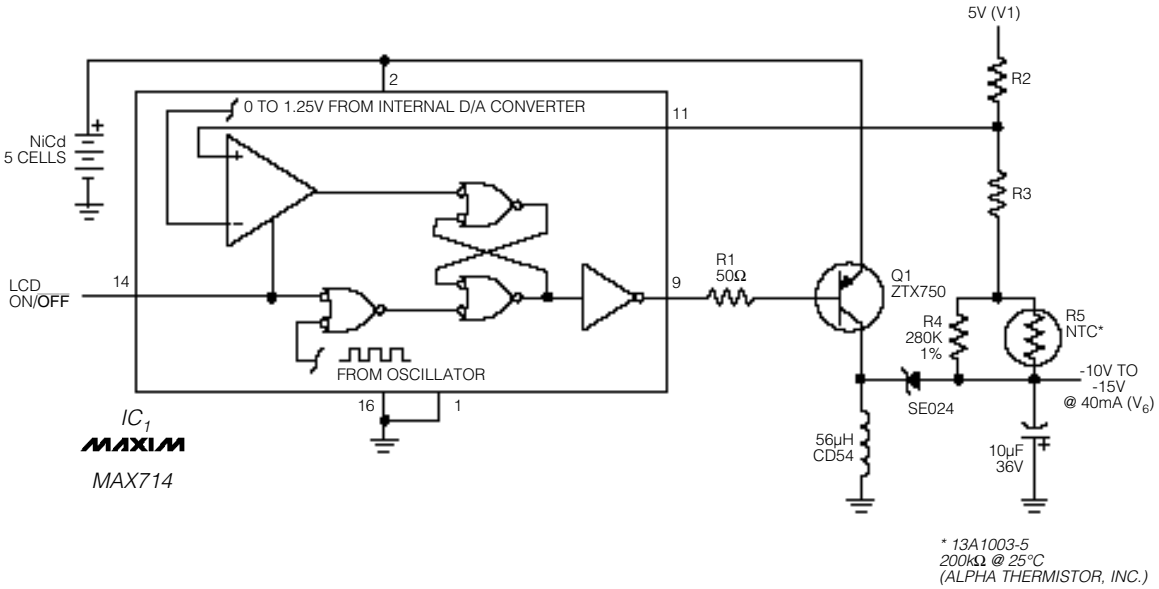

Figure 1. *The negative-tempco resistor R5 modifies feedback in this switching regulator, resulting in a negative output voltage that varies with temperature. With properly chosen resistor values (see text) the circuit produces a temperature-compensated bias voltage that assures constant contrast in an LCD.*